IN THE CLAIMS:

Amend the claims as indicated below.

Claim 83 (canceled)

84. (New) A content addressable memory (CAM) device comprising:

a plurality of CAM blocks, each comprising at least one storage partition, wherein a storage partition comprises one or more configurable portions of one or more CAM blocks, and wherein a class code specifies a particular storage partition;

a block select circuit coupled to the plurality of CAM blocks, wherein the block select circuit receives a class code signal that indicates a storage partition that will participate in a CAM operation and outputs a configuration signal to each of the plurality of CAM blocks that indicates a CAM block configuration corresponding to the received class code signal; and

a plurality of block flag circuits each coupled to the block select circuit and to one of the plurality of CAM blocks, wherein each block flag circuit receives a configuration signal and a plurality of row flag signals, wherein the plurality of row flag signals indicate results of the CAM operation on a row basis, and wherein each block flag circuit outputs a block flag signal that indicates a result of the CAM operation within the coupled CAM block for the storage partition indicated by the class code signal.

85. (New) The CAM device of claim 84, wherein the block select circuit further outputs a block select signal for each of the plurality of CAM blocks, wherein the block select signal indicates whether a CAM block is part of the storage partition indicated by the class code signal.

86. (New) The CAM device of claim 85, wherein if the CAM block is not part of the storage partition indicated by the class code signal, the CAM block does not participate in the CAM operation and block flag signal does not indicate a result of the CAM operation within the coupled CAM block.

87. (New) The CAM device of claim 84, further comprising:

an operation select signal received by each of the block flag circuits that indicates the CAM operation to be performed, wherein the CAM operation comprises,

comparing at least one segment of each row to a comparand value; and

signaling, using a block flag signal coupled to a CAM block, a block match condition for the CAM block and class code if at least one comparison results in a match.

88. (New) The CAM device of claim 87, further comprising a global flag encoder circuit coupled to receive block flag signals from each of the plurality of CAM blocks, wherein when a block match condition is indicated for any of the plurality of CAM blocks having a same class code, the global flag encoder circuit outputs a device flag signal indicating the match condition.

89. (New) The CAM device of claim 84, further comprising:

an operation select signal received by each of the block flag circuits that indicates the CAM operation to be performed, wherein the CAM operation comprises,

examining valid signals for all segments of a CAM block coupled to a block flag circuit;

signaling, using a row flag signal, that a row is full when all the segments of a row

have valid entries; and

signaling, using a block flag signal, the CAM block is full when the row flags coupled to the CAM block indicate all rows are full.

90. (New) The CAM device of claim 89, further comprising a global flag encoder circuit coupled to receive block flag signals from each of the plurality of CAM blocks, wherein when all CAM blocks with a same class code are indicated to be full, the global flag encoder circuit outputs a device flag signal indicating a full condition.

91. (New) The CAM device of claim 84, wherein the CAM block configuration comprises a block width and a block depth.

92. (New) A content addressable memory ("CAM") device comprising:

a plurality of CAM blocks comprising a plurality of configurable storage partitions, wherein a storage partition is specified by a class code;

a block select circuit that receives a class code signal indicating a class code of a storage partition that will participate in a CAM operation and generates a configuration signal for each CAM block, wherein the configuration signal indicates a storage partition configuration corresponding to the class code; and

a plurality of block priority encoder circuits each coupled to one of the plurality of CAM blocks, wherein a block priority encoder circuit coupled to a CAM block receives a configuration signal for the coupled CAM block and generates a block index for the coupled CAM block that indicates a CAM address in the coupled CAM block based on the CAM operation performed and on the class code.

93. (New) The CAM device of claim 92, further comprising a global priority encoder circuit that receives a plurality of block indices and a plurality of block flag signals, wherein a block flag signal indicates a result of the CAM operation performed, and wherein the global priority encoder outputs a device index that indicates a CAM address in one of the plurality of CAM blocks based on the CAM operation performed and on the class code.

94. (New) The CAM device of claim 92, wherein the CAM operation comprises:

a compare operation, wherein the block index indicates a match address; and

a write operation, wherein the block address indicates a free address.

95. (New) The CAM device of claim 94, wherein:

when the CAM operation is a compare operation, the device index indicates a highest priority match address; and

when the CAM operation is a write operation, the device index indicates a next free address.

96. (New) The CAM device of claim 92, wherein each of the plurality of block priority encoders further comprises a main priority encoder that monitors row flag signals that indicate a result of the CAM operation on a row segment basis.

97. (New) The CAM device of claim 96, wherein when the CAM operation is a compare operation, the main priority encoder monitors row flag signals to generate a row address that corresponds to an address of a highest priority row of a CAM block having at least one row segment that matches the comparand.

98. (New) The CAM device of claim 97, wherein when the CAM operation is a write operation, the main priority encoder monitors row flag signals to generate a row address that corresponds to an address of a highest priority row of a CAM block that has at least one row segment that is not full.

99. (New) The CAM device of claim 98, wherein the block priority encoder further comprises select logic that receives the row address generated by the main priority encoder and the configuration signal, and selects a segment address associated with a row of CAM cells specified by the address of the highest priority row, and generates the block index.

100. (New) The CAM device of claim 92, wherein the configurable storage partitions are configurable into at least a specified width and a specified depth.